All-optical 3-bit Parity Checker on PhC platform

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Abstract
Research on all-optical logic devices has been increasingly sought after in recent decades because to their potential for high-speed computing and lossless communications. This article presents a 3-bit odd parity checker that utilizes a T-shaped photonic crystal waveguide based XOR gate. The T-shaped waveguide is formed on a photonic crystal by introducing line and point defects. The suggested design is simulated using the Finite-Difference Time-Domain (FDTD) approach, resulting in an estimated contrast ratio of 27.48 decibels (dB) and a response time in picoseconds, as it operates in the all-optical domain.
Index Terms- All-optical, Photonic crystal, Contrast ratio, T-shaped waveguide, FDTD.

1. INTRODUCTION

High speed computing and communication systems has been in much demand since the couple of decades, led the researchers to work towards implementation of all-optical signal processing schemes. Compared to the conventional O-E-O (Optical -Electrical - Optical) schemes, the all-optical counterpart highly increases the operational speed to *Tbps* and greatly reduces the power requirement [1]. Moreover these schemes are capable to handle signals of large bandwidth without O-E-O conversion [2]. All-optical gates play an important role in the development of high speed telecommunication networks and systems as well as in optical computing modules. In many ways these gates have been implemented using Semiconductor Optical Amplifiers (SOAs), MZI based on electro-optic effect, Optical fibers etc. But, most of these works are limited by speed, size and difficulty in performing chip-level integration. Recent advances in material science shows that Photonic Crystal (PhC) can be a better platform for the implementation of logic gates due to its unique features like compactness, low power consumption, high speed, and ease of chip level integration.

Photonic crystal is such a feasible platform in which the devices can be constructed with miniaturized dimensions of light wavelengths being confined. So far, the logic gates have been reported with several phenomena such as interference [2-4], resonance [5], self-collimation [6], and both resonance and interference [7]. As per the best of our knowledge, the interference based designs provide high speed output at higher ON to OFF contrast ratio. So far in the literature, interference based designs are reported with higher contrast ratio.

In this article, the XOR and OR logic gates are proposed with T-shaped photonic crystal waveguides. The symmetric waveguide branches are maintained at equal lengths and are designated as inputs, and the third input is considered as output. These XOR gates are interconnected to define a 3-bit parity checker which determines the odd parity. The simulation and analysis of the proposed structures are done by using Finite Difference Time Domain (FDTD) method. The latter part of this article is organized with the design of XOR gates, and parity checker as follows. The design of XOR gates are discussed in section II followed by the implementation of parity checker in Section III. Finally, it is concluded in section IV.

2. XOR AND OR LOGIC GATES

In this section, T-shaped waveguides are mapped on to a PhC which consists of square-type lattice array of cylindrical *Si* rods with air base. The radius (r) of the *Si* rod and lattice constant (a) is $0.18a$ and 540 nm, respectively. Line defects are introduced to created T-shaped waveguides along with some point defects as directional rods as shown in Fig. 1.

In the waveguide, the symmetric branches are considered as inputs A and B while the other branch is output Y. Before using photonic crystal for the creation of waveguides, its Photonic Band Gaps (PBG) are calculated from the band diagram which is defined using Plane Wave Expansion (PWE) method, illustrated by Fig. 2. According to the band diagram, the Photonic Crystal which is used for the design of T-shaped waveguide supports two PBG's of TE mode and one PBG of TM mode. Only one band is selected that ranges from 0.2993 (a/λ) to 0.4414 (a/λ) i.e., 1223 nm to 1804 nm, and this band accommodates 1550 nm where the loss is very less. PBG in PhC varies with change in the material used, shape of the rods or holes in the crystal, type of the lattice and so on. Basically, in the analysis, photonic crystals are always considered to be perfect periodic structures.

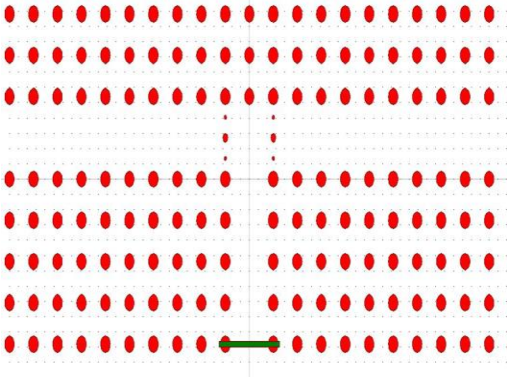


Fig. 1 Lattice structure of T-shaped PhC waveguide

Same way as doping in semiconductor materials for the design of electronic devices, photonic crystals are also subjected to the insertion of defects to implement specific optical functions. Defect is nothing but the change in structural parameters of the crystal such as change in the material used, shape of the rods or holes in the crystal, type of the lattice etc. These defects may be localized or extended which causes disruption in the periodicity of the PhC. As soon as the periodicity of the PhC is disrupted due to the insertion of defects, the translational symmetry would disappear and the Bloch modes will no longer be the solutions of Maxwell's equations. The PhC with point and line defects can be used as a resonator and a waveguide, respectively, also a uniform PhC can be used as a reflector as it offers PBG.

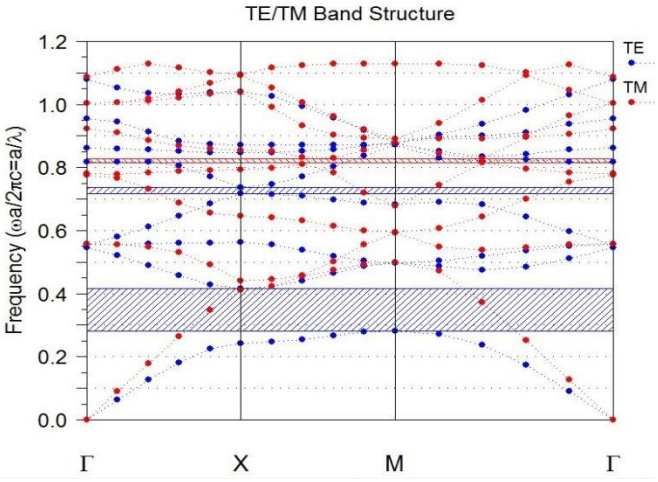


Fig. 2 Band diagram of the uniform photonic crystal

The above T-shaped waveguide with a phase difference between the inputs A and B at 180º and 0º operates as XOR and OR gates, respectively. In these gates, mostly light intensity is treated as logic levels. Light is treated as logic '1'

and no light is treated as logic '0' at the input. At the output, magnitude of light intensity is considered in such a way that a minimum contrast ratio (CR) of 5dB can be observed. The CR is such a metric with which one can differentiate logic '1' from logic '0', and it is given as CR = 10 log(P_1/P_0), where P_1 and P_0 are the transmission values of logic '1' and logic '0', respectively.

Simulation Results: In order to simulate the structures, input light is launched with Gaussian profile at 1550 nm. Simulation is done with perfectly matched boundary conditions into consideration which absorb electromagnetic waves and circumvent the boundary reflections. The (*x*,*z*) is the wave propagation plane and the polarization of the magnetic field is considered to be in parallel with *Si* rods. The FDTD method should solve the Maxwell's equations in both space and time fields. To guarantee the simulation convergence, $\Delta x < \lambda/10$ and $\Delta z < \lambda/10$, where *x* and *z* axes are the coordinates of horizontal and vertical directions, respectively. To achieve stability in the simulations, the space and the time grids are chosen such that the Courant condition [8] given below is satisfied

$$c\Delta t < \frac{1}{\sqrt{(\Delta x)^{-2} + (\Delta z)^{-2}}} \quad (1)$$

where c is the speed of light in free space.

As discussed previously, the T-shaped PhC waveguide can be used as XOR and OR gate by maintaining the phase difference of 180º and 0º, respectively. The electric field distribution of XOR and OR gates is shown in Fig. 3, and the output transmission is shown in Fig. 4. The transmission is tabulated in Table 1.1 from the calculated contrast ratio obtained is 42.09 dB.

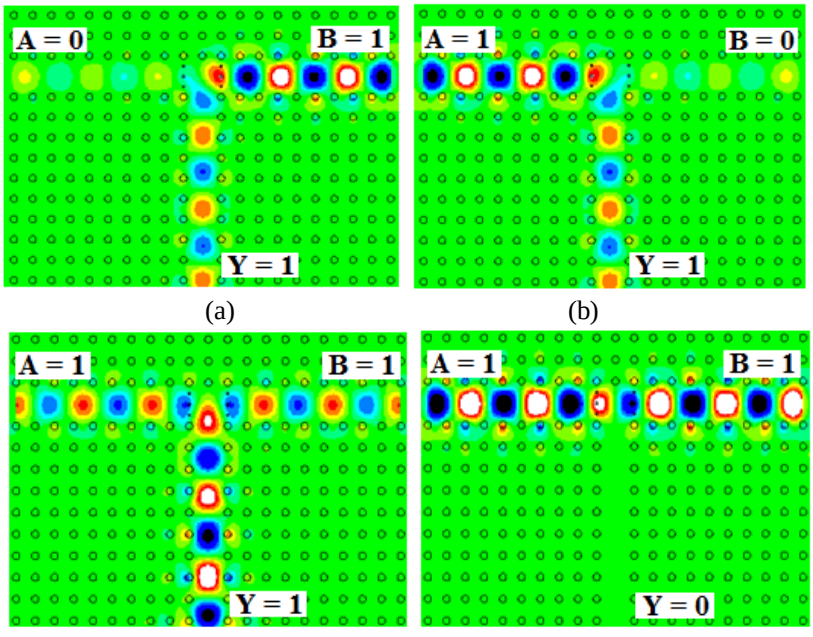


Fig. 3 Electric field distribution of T-shaped PhC waveguide at a) AB = 01, b) AB = 10, c) AB = 11 of XOR gate, d) AB = 11 of OR gate

Table 1.1 Performance of XOR gate

A	B	Y*(Pout/Pi)*
0	0	0
0	1(180º)	0.486
1	0	0.486
1	1(180º)	0.00003

3. 3-BIT PARITY CHECKER CIRCUIT

The parity checker circuit is derived from the interconnection of XOR gates as shown in Fig. 5(a, top), and it is used

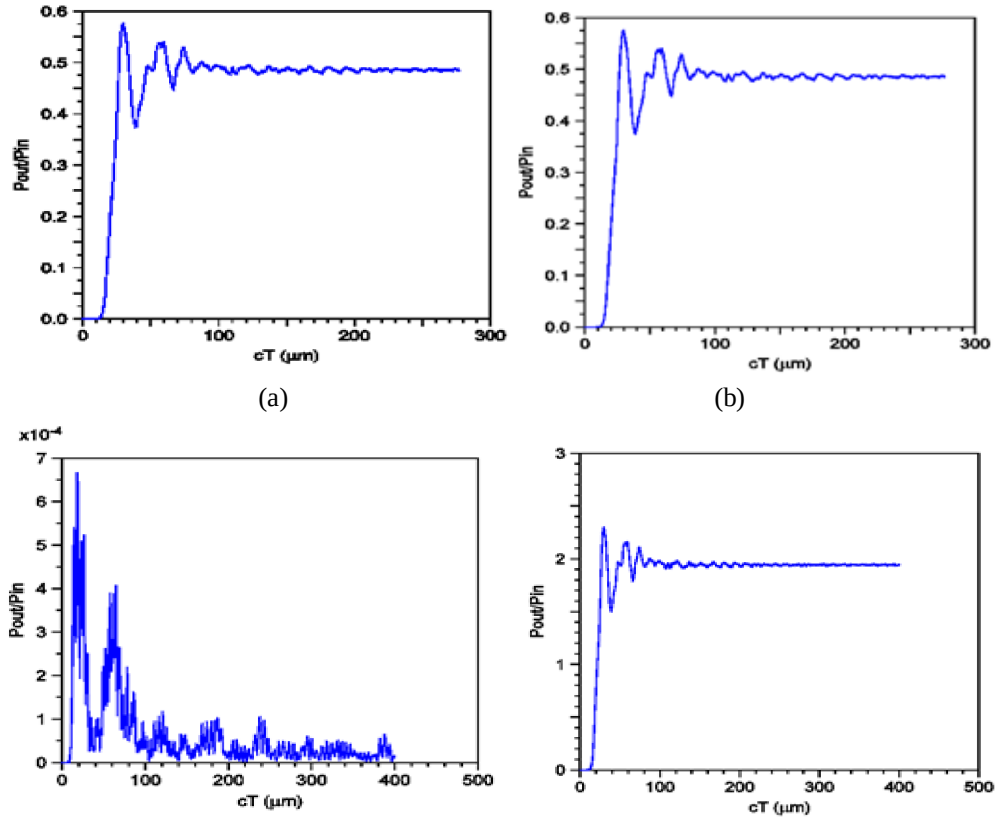
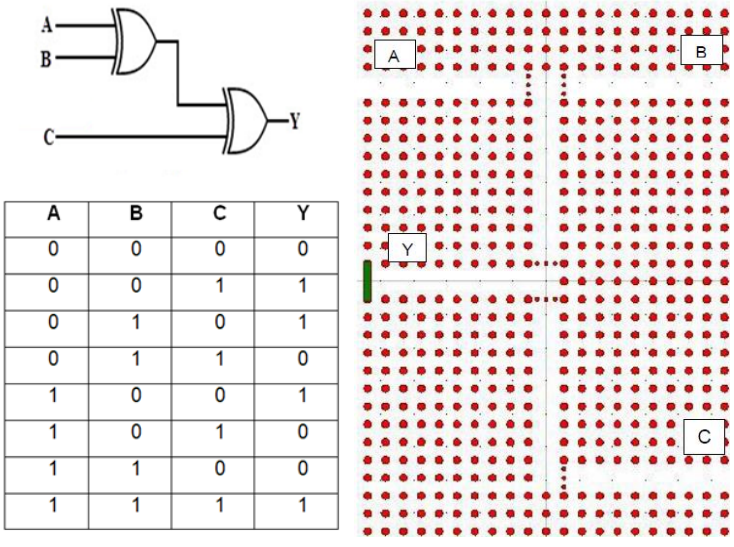


Fig. 4 Output transmission at a) AB = 01, b) AB = 10, c) AB = 11 of XOR gate, d) AB = 11 of OR gate



A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(a) (b)

Fig. 5 a) Schematic circuit (top) and functional table(bottom), and b) lattice structure of 3-bit parity checker

to check odd parity illustrated by Fig. 5(a, bottom). Two T-shaped waveguides are connected with each other as in the schematic circuit. The other branch of second T-shaped waveguide is extended to accommodate input C, illustrated in Fig. 5(b), so that proper interference can happen. The additional defects at the L-bend of the input C is taken in order to maintain the equal effect over the input light. The phase at the input of logic gates is varied to achieve the required output. The 180º phase at inputs A and C is maintained except the input combination '101' wherein one among them is kept at zero phase in order to have destructive interference.

The proposed 3-bit parity checker is simulated for all the input combinations to verify the output. As per the functional table shown in Fig. 5(a, bottom), the output is observed with light intensity of appropriate magnitude as

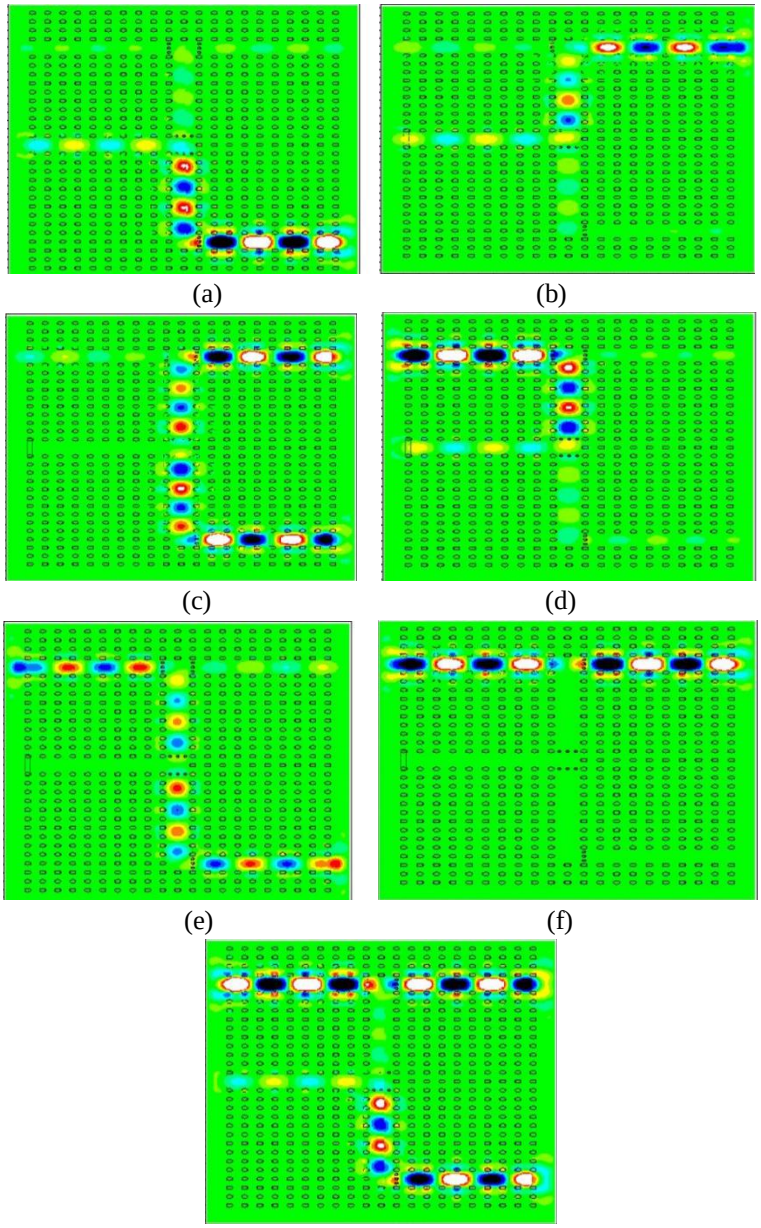
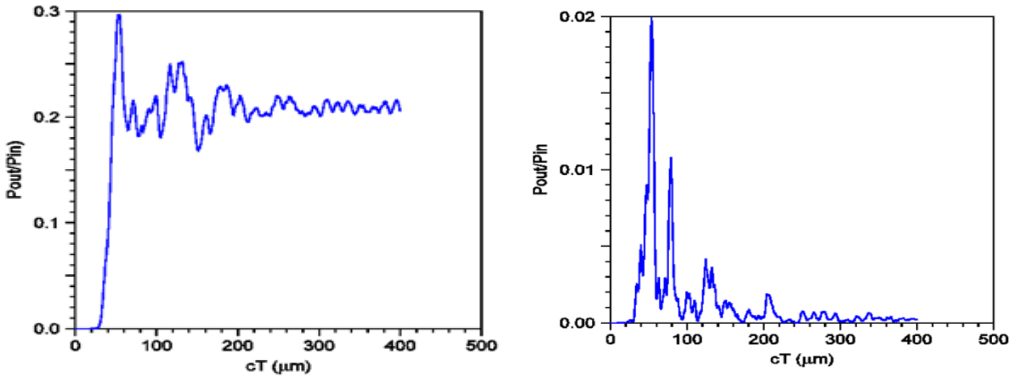


Fig. 6 Electric field distribution of the 3-bit parity checker with ABC at a) 001, b) 010, c) 011, d) 100, e) 101, f) 110, and g) 111



(a) (b)

Fig. 7 The output transmission for a) logic '1' and b) logic '0'

logic '1' and negligible intensity as logic '0'. The intensity levels are maintained in such a way that the contrast ratio can be minimum of 5dB. The electric field distribution for all the inputs are illustrated in Fig. 6 except the first one for which all the inputs are zero (i.e., no light). The output transmission for logic '0' and logic '1' is also observed in Fig. 7. The output transmission obtained for logic '0' and logic '1' is observed as 0.0004 and 0.224. respectively from which the contrast ratio is 27.48 dB.

Although the output transmission (intensity) at the output of the proposed design is low at 0.224 to be recognized as logic '1', it is considered as such. Because, the logic structure being proposed here are assumed to be maintained with a contrast ratio of at least above 5dB, which is the minimum value reported in the literature so far.

4. CONCLUSION

In this article, a 3-bit parity checker has been proposed with XOR gate defined by T-shaped photonic crystal waveguide. It determines the odd parity of the applied inputs which are of optical signals. The XOR gate also works as OR gate with zero phase difference. The XOR gates have been interconnected to define 3-bit parity checker with a contrast ratio of 27.48 dB with a response time in picoseconds as the inputs are optical.

REFERENCES

1. S. Zeng, Y. Zhang, B. Li, and EY-B. Pun, "Ultra small optical logic gates based on silicon periodic dielectric waveguides," Photon. Nanostruct. vol. 8, pp. 32-37, Jan. 2010.

2. P. Rani, K. Yogita, and R.K. Sinha, " Realization of AND gate in Y-shaped photonic crystal waveguide," Opt. Commun. vol. 298–299, pp. 227-231, Mar. 2013.

3. Z-H. Zhu, W-M. Ye, J-R. Ji, X-D. Yuan, and C. Zen, "High-contrast light-by-light switching and AND gate based on nonlinear photonic crystals," Opt. Express, vol. 14, pp. 1783–1788, Mar. 2006.

4. E. Shaik, K. Satamraju, R. Shaik and M. Vasantha Lakshmi, "Interference based all-optical 4 x 2 Encoder," International Journal of Recent Technology and Engineering, vol. 7(4), pp. 338-341, Nov. 2018.

5. B. Riadh, B. Afrah, and E. Hatem, "Design of silicon-based two-dimensional photonic integrated circuits: XOR gate," IET Optoelectron. vol. 7, pp. 25–29, Nov. 2013.

6. X.S. Christina and A.P. Kabilan, "Design of optical logic gates using self-collimated beams in 2D photonic crystal," Cryst. Photonic Sens. vol. 2, pp. 173-179, Apr. 2012.

7. A. Salmanpour, S. Mohammednejad, and A. Bahrami, " All-optical photonic crystal AND, XOR and OR logic gates using nonlinear Kerr effect and ring resonators," J. Moder. Opt. vol. 62, pp. 693-700, Feb. 2015.

8. C.J. Wu, C.P. Liu, and Z. Ouyang, "Compact and low-power optical logic NOT gate based on photonic crystal waveguides without optical amplifiers and nonlinear materials," Appl. Opt. vol. 51, pp. 680-685, Feb. 2012.